

WHAT IS CLAIMED IS:

1. A solid state image pickup device comprising:
an image pickup unit including plural
photoelectric conversion elements; and

5 a reference clock generation circuit for
determining the timing of a drive pulse;

wherein said image pickup unit and said reference
clock generation circuit are formed in a same
semiconductor chip.

10 2. A solid state image pickup device according to
claim 1, further comprising:

a drive pulse generation circuit for driving said
image pickup unit;

15 wherein said drive pulse generation circuit is
formed in said semiconductor chip.

20 3. A solid state image pickup device according to
claim 1, wherein a preliminary control circuit for
driving said image pickup unit in a predetermined
preliminary operation mode is formed on said
semiconductor chip.

25 4. A solid state image pickup device according to
claim 2, wherein a preliminary control circuit for
driving said image pickup unit in a predetermined
preliminary operation mode is formed on said

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semiconductor chip.

5. A solid state image pickup device according to claim 3, wherein a switch for supplying the drive pulse generation circuit of said semiconductor chip selectively with a reference clock signal from said reference clock generation circuit incorporated in said semiconductor chip and a drive mode control clock signal from said preliminary control circuit, or a reference clock signal and a drive mode control clock signal from the exterior of said semiconductor chip, is formed on said semiconductor chip.

6. A solid state image pickup device according to claim 4, wherein a switch for supplying the drive pulse generation circuit of said semiconductor chip selectively with a reference clock signal from said reference clock generation circuit incorporated in said semiconductor chip and a drive mode control clock signal from said preliminary control circuit, or a reference clock signal and a drive mode control clock signal from the exterior of said semiconductor chip, is formed on said semiconductor chip.

7. A solid state image pickup device according to claim 3, wherein said device has a preliminary operation mode for operating said image pickup unit in

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synchronization with the reference clock signal and the preliminary operation control clock signal from said reference clock generation circuit and said preliminary operation control circuit integrated in said semiconductor chip, and a main operation mode for operating said image pickup unit in synchronization with the reference clock signal and the drive mode control clock signal from the exterior of said semiconductor chip, wherein the operation in said semiconductor chip is executed with a power consumption lower in said preliminary operation mode than in said main operation mode.

8. A solid state image pickup device according to claim 4, wherein said device has a preliminary operation mode for operating said image pickup unit in synchronization with the reference clock signal and the preliminary operation control clock signal from said reference clock generation circuit and said preliminary operation control circuit integrated in said semiconductor chip, and a main operation mode for operating said image pickup unit in synchronization with the reference clock signal and the drive mode control clock signal from the exterior of said semiconductor chip, wherein the operation in said semiconductor chip is executed with a power consumption lower in said preliminary operation mode than in said

main operation mode.

9. A solid state image pickup device provided
with a solid state image pickup chip including an image
pickup unit and a drive pulse generation circuit chip
including a drive pulse generation circuit for driving
said image pickup unit, wherein a reference clock
generation circuit for determining the timing of the
drive pulse is formed in said drive pulse generation
circuit chip.

10. A solid state image pickup device according
to claim 9, wherein a preliminary control circuit for
driving said state image pickup chip in a predetermined
drive mode is formed in said drive pulse generation
circuit chip.

11. A solid state image pickup device according
to claim 10, wherein a switch for supplying the drive
pulse generation circuit of said semiconductor chip
selectively with a reference clock signal from said
basic clock generation circuit incorporated in said
reference pulse generation circuit chip and a drive
mode control clock signal from said preliminary control
circuit, or a reference clock signal and a drive mode
control clock signal from the exterior of said
semiconductor chip, is formed on said drive pulse

generation circuit chip.

5 12. A solid state image pickup device according
to claim 10, wherein said device has a preliminary
operation mode for operating said image pickup unit in
synchronization with the reference clock signal and the
preliminary operation control clock signal from said
reference clock generation circuit and said preliminary
operation control circuit integrated in said drive
10 pulse generation circuit chip, and a main operation
mode for operating said image pickup unit in
synchronization with the reference clock signal and the
drive mode control clock signal from the exterior of
said chip, wherein the operation in said chip is
15 executed with a power consumption lower in said
preliminary operation mode than in said main operation
mode.

20 13. A solid state image pickup device
comprising:

an image pickup unit including plural
photoelectric conversion elements;

a drive pulse generation circuit for driving said
image pickup unit;

25 a reference pulse generation circuit for
determining the timing of a drive pulse;

a first control circuit for controlling the

operation mode of said drive pulse generation circuit;

a second control circuit for controlling the
operation mode of said drive pulse generation circuit;
and

5 a switch for connecting said first control circuit
or said second control circuit to said drive pulse
generation circuit.

10 14. A solid state image pickup device according
to claim 13, wherein said switch is adapted to turn off
the power supply to said first or second control
circuit which is not connected to said drive pulse
generation circuit.

15 15. A solid state image pickup device according
to claim 13, wherein said first control circuit
functions with a lower electric power consumption than
in said second control circuit.

20 16. A solid state image pickup device according
to claim 15, further comprising:

a signal processing unit for executing image
processing on the signal from said image pickup unit;
wherein said signal processing unit is controlled
25 by said second control circuit.

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